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METHOD FOR FABRICATING A PLATE-SHAPED STRUCTURE, IN PARTICULAR  
FROM SILICON, USE OF SAID METHOD, AND PLATE-SHAPED STRUCTURE THUS  
PRODUCED, IN PARTICULAR FROM SILICON

By:

Michel Bruel

Attorney Docket No.: 5310-09500

Customer No.: 35690  
Eric B. Meyertons  
Meyertons, Hood, Kivlin, Kowert & Goetzel, P.C.  
P.O. Box 398  
Austin, Texas 78767-0398  
Ph: (512) 853-8800

**BACKGROUND OF THE INVENTION**

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1. Field of the Invention

5           The present invention relates to the field of fabricating multi-layered plates, and to fabricating thin wafers.

2. Description of the Relevant Art

10           In the microtechnology field, in particular in micro-electronics and opto-electronics, it is normal to use silicon wafers joined to an insulating layer, and more particularly structures comprising an insulating layer interposed between a substrate formed from silicon and a superstrate formed from silicon.

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## SUMMARY OF THE INVENTION

The present invention aims to improve current techniques and structures, thereby improving performance and diversifying applications.

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In a first aspect, the present invention concerns a method for fabricating a structure in the form of a plate comprising at least one substrate, a superstrate and at least one intermediate layer interposed between the substrate and the superstrate.

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According to the present invention, said method consists in selecting an intermediate layer comprising at least one base material having distributed therein atoms or molecules termed extrinsic atoms or molecules which differ from the atoms or molecules of the base material, and applying a heat treatment to said structure so that, in the temperature range of said heat treatment, the intermediate layer is plastically deformable, and the presence of the selected extrinsic atoms or molecules in the selected base material causes the irreversible formation of micro-bubbles or micro-cavities in the intermediate layer.

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According to the present invention, the heat treatment preferably produces micro-bubbles or micro-cavities which weaken said intermediate layer.

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According to the present invention, the heat treatment preferably produces a rupture of said intermediate layer and, as a result, separation of the substrate and the superstrate.

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The present invention also provides a method for separating the substrate and superstrate in the structure obtained by the above method.

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In a variation of the present invention, said separation method may consist in applying forces between the substrate and the superstrate to bring about the rupture of the intermediate layer between the substrate and the superstrate due to the presence of said micro-bubbles or micro-cavities.

In a further variation of the present invention, said separation method may consist in chemically attacking the intermediate layer to at least partially remove said intermediate layer between the substrate and the superstrate due to the presence of said micro-bubbles or micro-cavities.

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According to the present invention, the substrate and the superstrate may advantageously be formed from monocrystalline silicon and the intermediate layer may advantageously be formed from doped silica.

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The present invention also concerns a method for fabricating silicon wafers which consists in producing a structure in the form of a plate comprising a substrate formed from silicon, a superstrate formed from silicon and a dielectric intermediate layer comprising at least one base material having distributed therein atoms or molecules termed extrinsic atoms or molecules which differ from the atoms or molecules of the base material; then applying a heat treatment to said structure so that, in the temperature range of the heat treatment, the intermediate layer is plastically deformable and so that the presence of the selected extrinsic atoms or molecules in the selected base material causes the irreversible formation of micro-bubbles or micro-cavities in the intermediate layer.

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In accordance with the present invention, said base material is preferably silica and the extrinsic atoms are preferably atoms of phosphorus and/or boron, thus forming an intermediate layer of phospho-silicate glass (P.S.G.) or boro-phospho-silicate glass (B.P.S.G.).

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In accordance with the present invention, the concentration of phosphorus may advantageously be in the range from 6% to 14%.

In accordance with the present invention, the concentration of boron may advantageously be in the range from 0% to 4%.

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In accordance with the present invention, the heat treatment is preferably carried out at a temperature in the range from 900°C to 1200°C.

In accordance with the present invention, the method may advantageously consist, prior to said heat treatment, in carrying out an operation for depositing said intermediate layer on the substrate, or respectively the superstrate, and attaching the superstrate, or respectively  
5 the substrate, to said intermediate layer by molecular wafer bonding.

In accordance with the present invention, the method may advantageously comprise a supplemental step for reducing the thickness of the substrate.

10 In accordance with the present invention, on said intermediate layer side, the substrate and the superstrate may advantageously respectively comprise a thermal silicon oxide.

In accordance with a variation of the present invention, the method may advantageously consist in exerting forces on said structure in a manner such that rupture of  
15 said intermediate layer is brought about, resulting in separation of the substrate and superstrate due to the presence of said micro-bubbles or micro-cavities to obtain a wafer constituted by the substrate and/or a wafer constituted by the superstrate.

In accordance with a variation of the present invention, the method may  
20 advantageously consist in chemically attacking said intermediate layer of said structure to bring about separation of the substrate and superstrate due to the presence of said micro-bubbles or micro-cavities to obtain a silicon wafer constituted by the substrate and/or a silicon wafer constituted by the superstrate.

25 In accordance with the present invention, the method may advantageously consist in producing projecting portions in the substrate and/or the superstrate on said intermediate layer side.

In accordance with the present invention, the projecting portions are preferably  
30 rectilinear and extend to the sides of the structure.

In accordance with the present invention, at least some of said micro-bubbles or micro-cavities are preferably open-celled and at least some thereof constitute channels.

5 The present invention also pertains to an application of the method to the fabrication of silicon on insulator (S.O.I.) plates for the fabrication of integrated electronic circuits and/or integrated opto-electronic circuits.

10 The present invention also pertains to a structure in the form of a plate comprising at least one substrate, a superstrate and at least one intermediate layer interposed between the substrate and the superstrate.

15 In accordance with the present invention, said intermediate layer comprises at least one base material having distributed therein atoms or molecules termed extrinsic atoms or molecules which differ from the atoms or molecules of the base material so that, under the effect of a heat treatment, the intermediate layer becomes plastically deformable and the presence of the selected extrinsic atoms or molecules in the selected base material causes the irreversible formation of micro-bubbles or micro-cavities in the intermediate layer.

20 In accordance with the present invention, the substrate and the superstrate are preferably formed from monocrystalline silicon and the intermediate layer is formed from doped silica.

25 In accordance with the present invention, the base material is preferably silica and the extrinsic atoms are preferably atoms of phosphorus or boron, thus forming an intermediate layer of phospho-silicate glass (P.S.G.) or boro-phospho-silicate glass (B.P.S.G.).

In accordance with the present invention, the concentration of phosphorus is preferably in the range from 8% to 14%.

30 In accordance with the present invention, the concentration of boron is preferably in the range from 0% to 4%.

In accordance with the present invention, the substrate and/or the superstrate preferably have portions projecting into said intermediate layer.

5 In accordance with the present invention, the projecting portions are preferably rectilinear and extend to the sides.

In accordance with the present invention, at least some of said micro-bubbles or micro-cavities are open-celled and at least some thereof constitute channels.

### **BRIEF DESCRIPTION OF THE DRAWINGS**

The present invention will be better understood from a study of structures and a mode  
5 of fabrication of such structures, described with reference to non-limiting examples shown in  
the accompanying drawings in which:

Fig. 1 shows a cross section of a structure in accordance with the invention, in an  
initial state;

Fig. 2 shows an exploded cross section of the structure of Fig. 1 during fabrication;

10 Fig. 3 shows a section of the structure of Fig. 1, in a subsequent fabrication step;

Fig. 4 and 5 show a section of the structure of Fig. 1 in a secondary state of  
fabrication; and

Fig. 6 shows a variation of the structure of Fig. 1.

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## **DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS**

Fig. 1 shows a structure 1 in the form of a plate which, for example, has a diameter of about two hundred millimeters.

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This structure comprises a substrate 2 in the form of a wafer, a superstrate 3 in the form of a wafer and an intermediate layer 4 interposed between the substrate 2 and the superstrate 3.

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In general, the intermediate layer 4 is formed from at least one base material having distributed therein atoms or molecules termed extrinsic atoms or molecules which differ from the atoms or molecules of the base material, and has a composition such that, when a suitable heat treatment is applied to the structure 1, micro-bubbles or micro-cavities, in particular of a gaseous phase, are irreversibly formed such that said intermediate layer 4 transforms to become spongy and, as a correlation, it is likely to increase in thickness.

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An example of an embodiment of a structure 1 will now be described with reference to Fig. 2.

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The substrate 2 may be constituted by a monocrystalline silicon wafer which may be several hundred microns thick, for example in the range from five hundred to a thousand microns.

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Optionally but preferably, a film 5 of thermal silicon oxide is then produced on one face of the substrate 2.

This film 5 may be produced in an oxidation furnace, at a temperature in the range from 950°C to 1100°C, and may have a thickness of about 0.5 micron.

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Next, a layer of silicon containing or doped with a high percentage of phosphorus and/or boron is deposited on the oxidized face 5 of superstrate 2 to obtain the intermediate

layer 4 composed of a material of the phospho-silicate glass (PSG) or boro-phospho-silicate glass (BPSG) type.

As an example, the percentage of phosphorus in the material constituting the  
5 intermediate layer 4 may be in the range from 6 to 14. Such a deposit may be produced using known techniques in deposition machines of the CVD, LPCVD or PECVD type.

The thickness of the intermediate layer 4 so constituted may be in the region of five  
10 microns.

Optionally but preferably, the surface of the intermediate layer 4 may undergo a  
chemical cleaning treatment, for example an RCA type chemical cleaning, which is known  
per se.

15 Optionally but preferably, before or after the cleaning treatment, a chemical-mechanical polishing (CMP) operation may be carried out on the intermediate layer 4.

In the same manner, the superstrate 3 may be constituted by a silicon wafer optionally  
having a film 6 of thermal silicon oxide and which has optionally undergone an RCA  
20 chemical cleaning treatment and optionally a chemical-mechanical polishing operation (CMP).

In a corresponding manner, the intermediate layer 4 may have been produced on the  
oxidized face 6 of the superstrate 3.

25 Thereafter, the substrate 2 and the superstrate 3 are assembled by placing the oxidized face 6 of the superstrate 3 in contact on the intermediate layer 4 to obtain molecular wafer bonding, optionally facilitated by the application of force, preferably point bearing forces, between the substrate 2 and the superstrate 3.

30 In order optionally to increase the interfacial bonding energy, a consolidating heat treatment may be applied to the assembled structure 1 employing conditions which do not

cause transformation of the intermediate layer 4, i.e. the formation of micro-bubbles or micro-cavities, as will be described below.

5 A structure 1 is thus obtained, composed of a substrate 2 formed from silicon and a superstrate 3 formed from silicon separated by an intermediate layer 4 formed from an electrically insulating material.

Referring to Fig. 3, it can be seen that the thickness of the superstrate 3 may be much smaller than the thickness of the substrate 2 and may be in the range from a fraction of a  
10 micron to several tens of microns.

Such a thin substrate 3 may initially be used to produce the structure 1 as described with reference to Fig. 2.

15 However, in a variation, such a thin superstrate 3 may be obtained by reducing the thickness of a thick superstrate 3 initially employed to produce the structure 1 as described with reference to Fig. 2. Such a reduction in thickness may be brought about using known grinding, chemical attack or chemical-mechanical polishing techniques and may also be obtained by a cleavage technique, for example SMART-CUT, a known commercial method  
20 necessitating the ionic implantation of protons in a dose of the order of  $5 \times 10^{16} \text{ cm}^{-2}$  into the superstrate 3 prior to carrying out molecular wafer bonding as discussed above.

An operation for reducing the thickness of the substrate 2 could also be carried out.

25 As can be seen in Fig. 4, the structure 1 may then undergo a heat treatment carried out in a furnace, for example at a temperature in the range from  $900^{\circ}\text{C}$  to  $1100^{\circ}\text{C}$ .

Regarding the selected materials mentioned above, applying such a heat treatment in the selected temperature range renders the intermediate layer 4 plastically deformable and  
30 causes the irreversible formation of a gas phase constituted by micro-bubbles or micro-cavities 7 in the intermediate layer and, as a correlation, an increase in the thickness of said layer 4.

The quantity and volume of the micro-bubbles or micro-cavities 7 depend on the composition of the intermediate layer 4 and the conditions of the heat treatment applied to the structure 1.

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As an example, starting from five microns, after treatment, the intermediate layer may have a thickness in the range from fifteen to twenty microns.

As can be seen in Fig. 5, the micro-bubbles or micro-cavities 7 may be of a volume  
10 such that they are open on the substrate 2 and/or superstrate 3 face side and furthermore, they may be mutually open to constitute channels which are open to the side ends of the intermediate layer 4.

As can be seen in Fig. 6, it may be particularly advantageous to produce projecting  
15 portions 8, which are preferably rectilinear, in the substrate 2 and/or in the superstrate 3, for example by etching, so that said projecting portions 8 constitute rectangular notches. This disposition may facilitate the appearance of micro-bubbles or micro-cavities 7, one running into another to constitute channels.

20 The structure 1 just described, containing micro-bubbles or micro-cavities 7 in its intermediate layer 4, may have many applications.

It may be used as is for the production of electronic or opto-electronic integrated circuits on the silicon superstrate 3, mounted on a thick substrate 2 via the intermediate layer  
25 4 which constitutes an electrical insulator, the capacitance between the superficial layer constituted by the superstrate 3 and the support layer constituted by the substrate 2 being particularly low because of the presence of micro-bubbles or micro-cavities 7.

In a further application example, the channels which are optionally but intentionally  
30 created in the intermediate layer 4 by the micro-bubbles or micro-cavities 7 may be used to circulate a cooling fluid between the substrate 2 and the superstrate 3 with the aim of cooling the structure 1.

In a further particularly advantageous application, the structure 1 containing micro-bubbles or micro-cavities 7 constitutes a releasable structure because the presence of the micro-bubbles or micro-cavities 7 in the intermediate layer 4 weakens the physical or chemical strength of this layer.

By applying forces between the substrate 2 and the superstrate 3 using any known means and, for example, by inserting a fine blade between the substrate 2 and the superstrate 3 or a jet of water under very high pressure, the intermediate layer 4 may be caused to rupture and thereby cause separation of the substrate 2, which then constitutes a wafer, and superstrate 3, which then constitutes a wafer, by rupture of the material of the intermediate layer 3 between the micro-bubbles or micro-cavities 7.

It is also possible to carry out a chemical attack of the intermediate layer 4 from its sides, for example using a solution of hydrofluoric acids, which can readily progress between the substrate 2 and the superstrate 3 due to the presence of micro-bubbles or micro-cavities 7.

Thus, starting from the structure 1 described with reference to Fig. 3, a thin silicon wafer constituted by the thin superstrate 3 is produced.

The thin silicon wafer 3 obtained may be fixed by one or the other of its faces to any final operating support formed from plastic, for example, to produce flexible electronic and/or opto-electronic circuits.

The present invention is not limited to the examples described above. Variations in the implementations are possible without departing from the scope of the invention defined in the accompanying claims.